Interference Signal Power Monitoring within Front-End Circuits of Wireless Receivers

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Abstract

With the growing density and variety of wireless devices in modern environments, the design of radio frequency (RF) receivers with improved robustness against unwanted interference signals has become increasingly important. Ongoing research addresses this challenge through the development of novel devices, circuits, and digital algorithms that enhance receiver performance. Within this context, this project supplements existing work on automatic calibration techniques based on signal power detection and digital control of analog RF front-end circuits. The project involved the investigation of how different signal waveforms affect the accuracy of power detection methods, experimental measurements using a power detector as part of a prototype setup, and the refinement of the current measurement setup to support more reliable and comprehensive characterization of interference suppression capabilities. The resulting measurements improved the precision and repeatability of power detection under varying waveform conditions, providing a more robust experimental foundation for validating automatic calibration algorithms and advancing the broader goal of building interference-resilient RF receivers.

Background

Modern wireless environments contain an increasing number of RF devices, resulting in greater interference between communication systems. Strong interfering signals can reduce receiver sensitivity, degrade signal quality, and limit overall system performance, making improved RF receiver resilience essential for applications such as Wi-Fi, cellular networks, IoT devices, and satellite systems. One promising solution is the Frequency Selective Limiter (FSL), an electronic device that blocks or attenuates signals exceeding a specified power threshold within a target frequency band. Ongoing research focuses on creating tunable FSLs and an automatic calibration method that combines signal power detection with digital control to continuously optimize analog RF front-end performance.

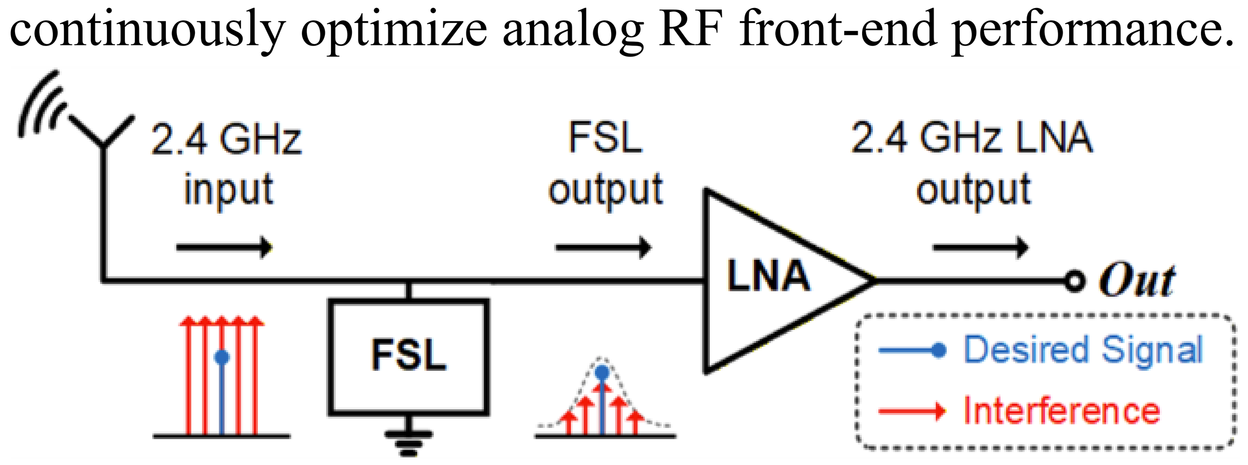


Figure 1: RF front-end with FSL and LNA for interference suppression [2].

This work supports the development of interference-resilient RF receivers by evaluating waveform-dependent power detection performance and improving the experimental measurement platform for future automatic calibration research.

Experimental Methods

Software and Hardware

- MXG N5183A Analog Signal Generator
- Arduino IDE
- Arduino Mega 2560 Rev3
- Radio Frequency Power Detector
- 5V DC Power Supply
- Programmable RF Attenuator
- AFG3252C Function Generator
- LTspice

Methods

A setup containing an attenuator, power detector, and Arduino microcontroller was constructed to mimic FSL tuning behavior. Using the Arduino, the attenuator was adjusted based on a dynamical control algorithm. Next, four different automatic calibration algorithms were developed and optimized to evaluate different performance tradeoffs.

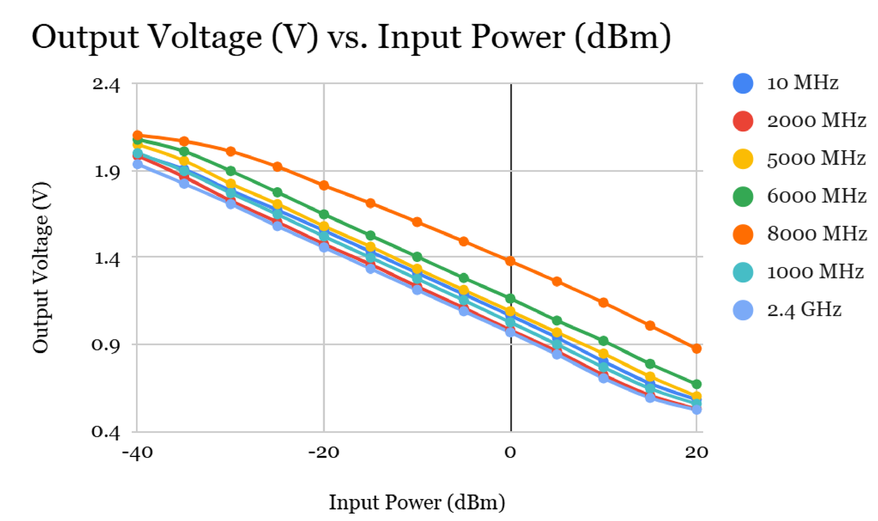
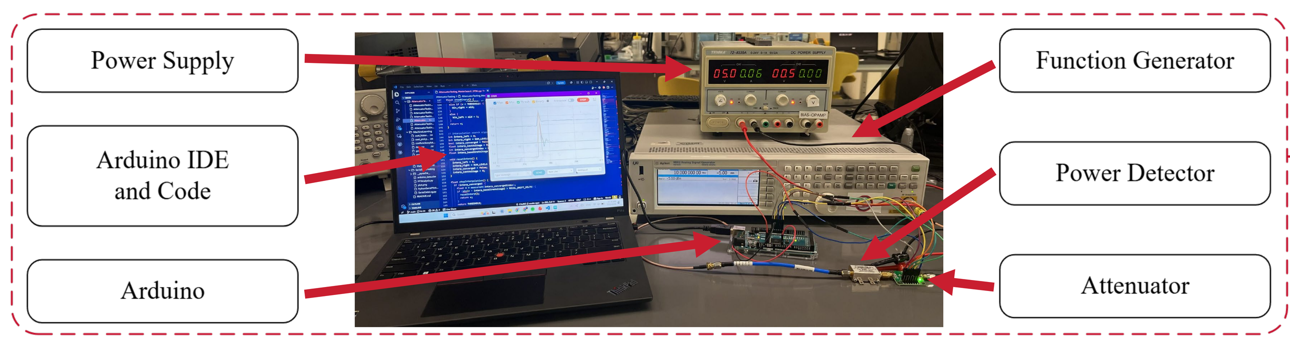


Figure 2: Power detector transfer function (V_{out} vs. P_{in}). Different output voltages were recorded using an Arduino analog pin with seven varied signal frequencies while adjusting input powers.



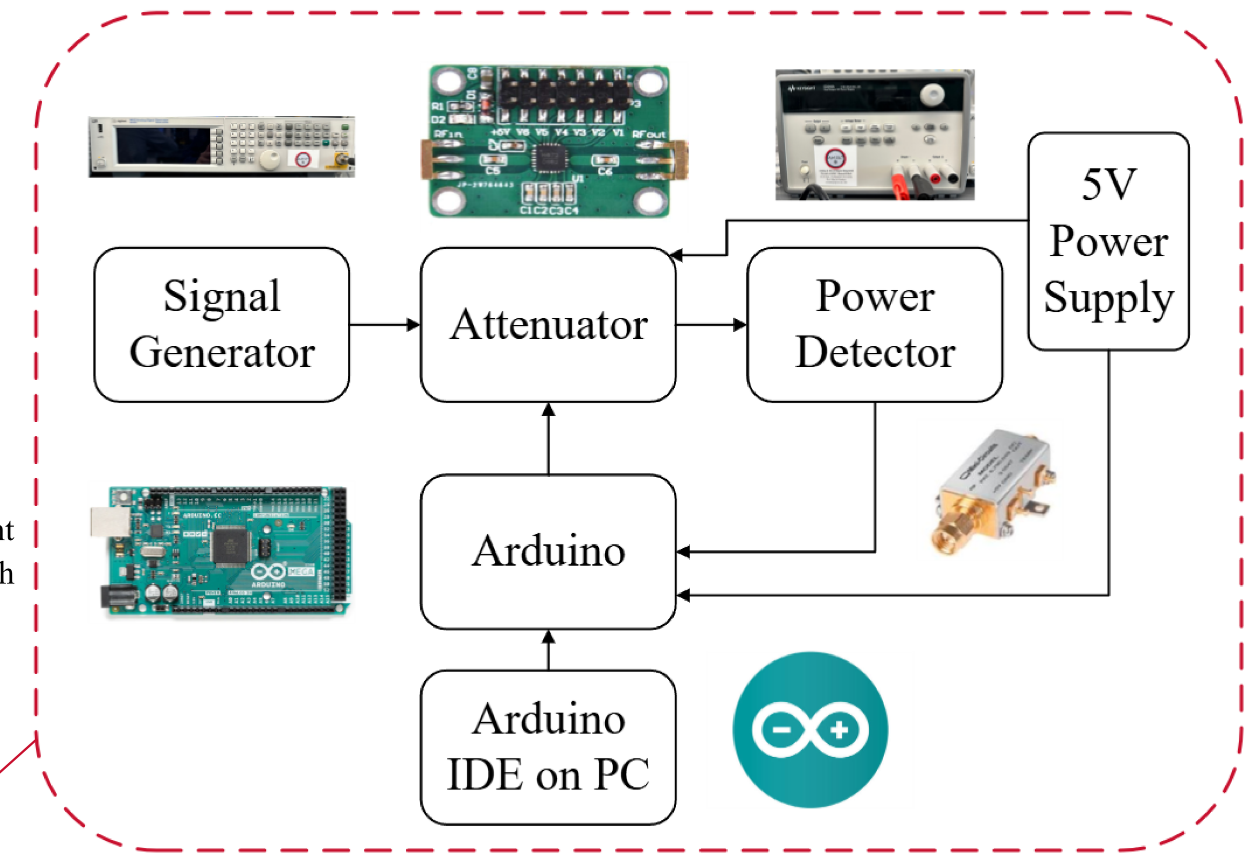


Figure 3: Experimental measurement setup. Feedback loop with power detector and Arduino control for attenuation selection based on input signal power.

Results

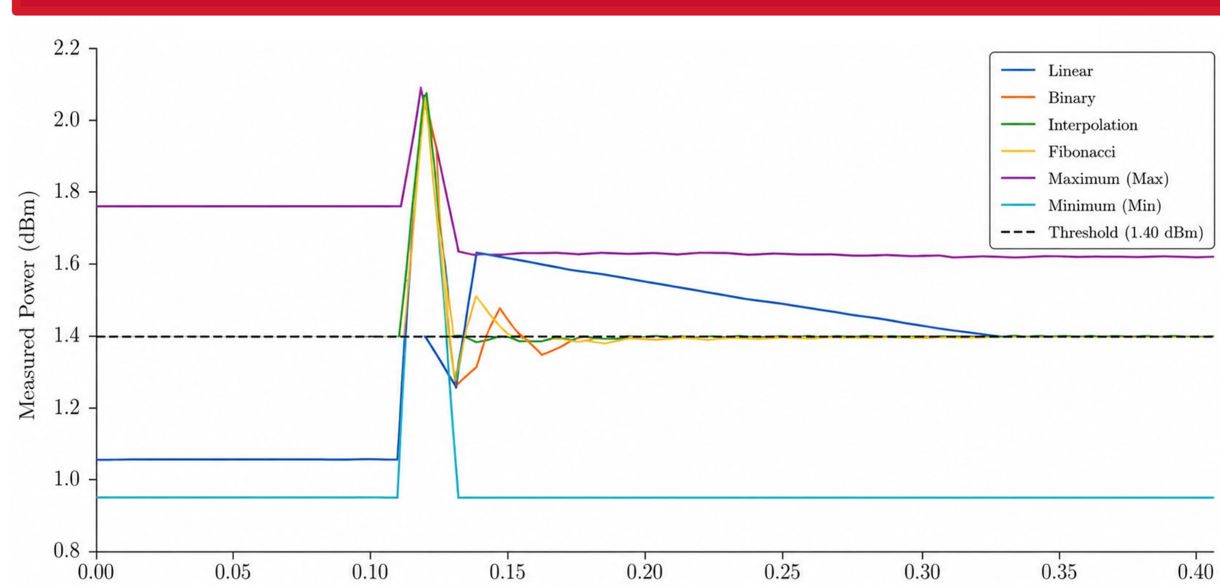


Figure 4: Search algorithm responses to input power changes during measurements with the power detector. Given a high-frequency signal of 5 dBm and 10 MHz, the Arduino processor simultaneously performed different search algorithms to control the programmable attenuator for the generation of an output voltage threshold of 1.4 dBm: linear (blue), binary (orange), interpolation (green), and Fibonacci (yellow)

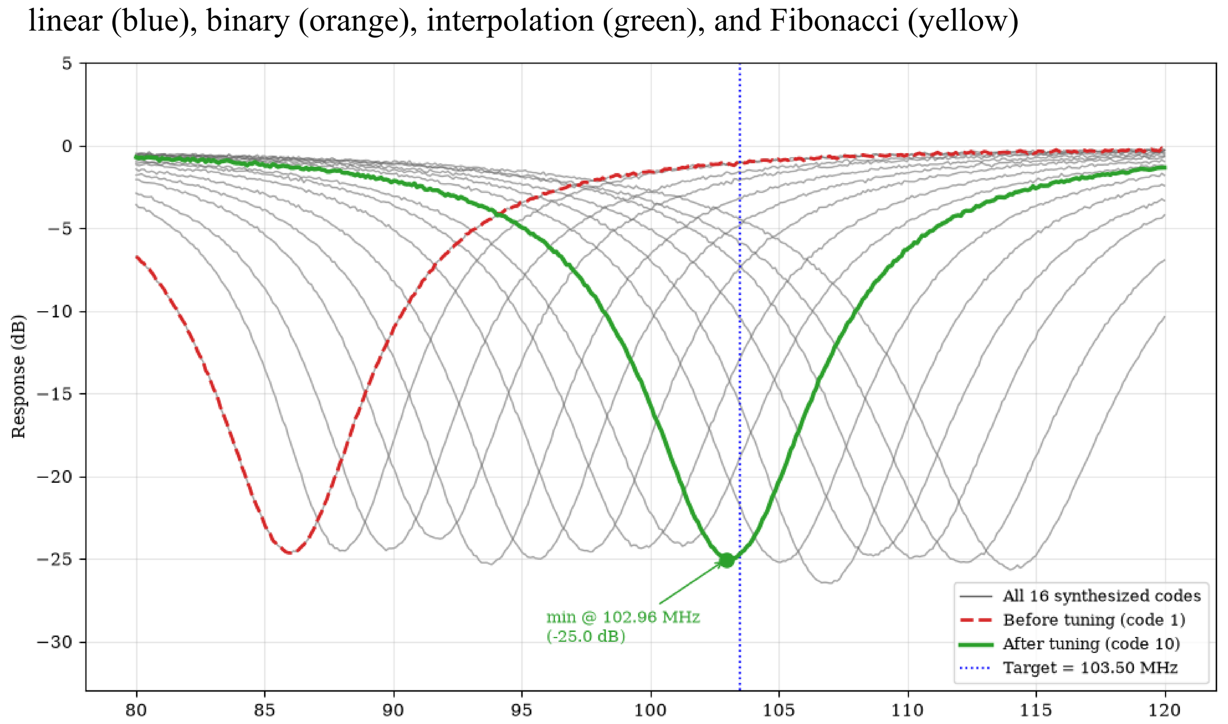


Figure 5: FSL auto-tuning model (synthesized codes) simulations: before vs. after. 16 synthesized code datasets of modeled FSL graphs were mapped to optimize a potential FSL frequency of 103.50 MHz. Code 1 (red) is a demonstration of the FSL output before tuning. Code 10 (green) is the fully optimized code. The target 103.50 MHz is outlined in blue.

Table 1: Comparison of Search Algorithms for Automatic Calibration

Method	Avg. Time (ms) to Settle within 1%	Avg. Iteration	Avg. Time of Each Iteration (ms)	Avg. Error (%)
Interpolation	90.5	5.36	16.88	0.38
Binary	278.29	4.43	62.82	0.30
Fibonacci	384.5	5.79	66.41	0.41
Linear	2445.93	34.57	70.75	0.67

- Interpolation provided best balance of speed and accuracy
- Binary search required the fewest iterations
- Linear search exhibited poorest performance
- The FSL-tuning model emulates the automatic search as part of the optimization process

Scan for full video demonstration

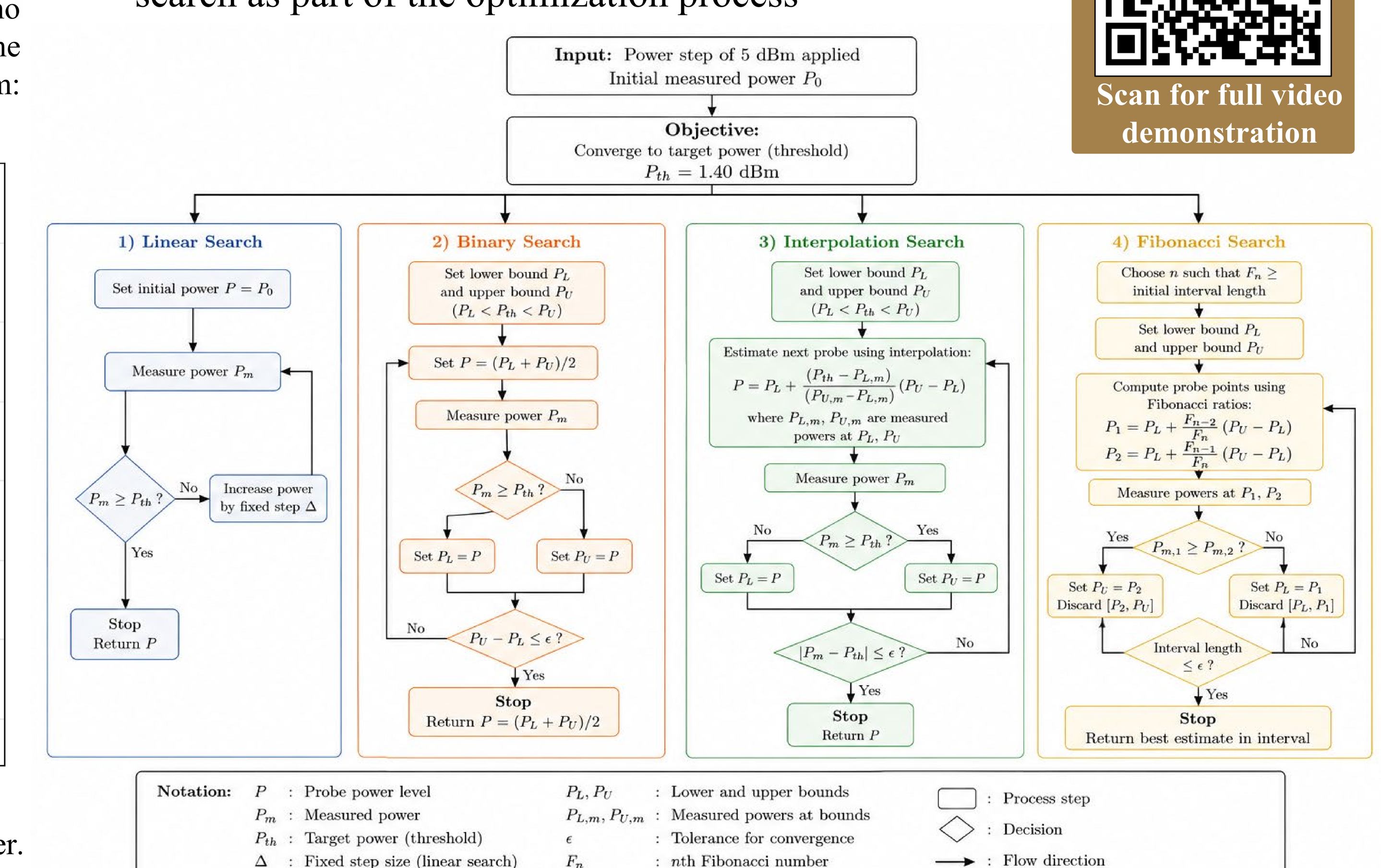


Figure 6: Flowchart of search algorithms for automatic calibration. Each algorithm iteratively probes and updates control settings until the measured power converges to the target power (P_{th} = 1.40 dBm).

Conclusion and Future Work

This research demonstrates that adaptive search algorithms can effectively automate RF power-based calibration of FSLs, significantly reducing calibration time while maintaining high accuracy. Among the evaluated methods, interpolation search achieved the best overall balance of convergence speed and precision, while binary search minimized the number of required iterations. The successful implementation of automatic FSL tuning further validates the feasibility of replacing manual calibration with intelligent search-based optimization. Future work will focus on evaluating the system across a wider range of operating conditions, implementing the framework on dedicated embedded hardware, and exploring hybrid and machine learning-assisted search techniques to further improve calibration speed and robustness.

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